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Investigation of Detection Circuits for Fast Level Detection within a SDARS Diversity System

The accurate signal level detection allows a faster antennas switching process. To achieve a stable signal level and a suitable signal variation range at the detection module output it was used a two steps processing of the detected signal. Very important is the detection period that have to be as short as possible. The detection module requests are: low-noise components, small time constants and the parasitics capacity reducing.

Keywords: *signal, detection circuts, SDARDS system*

1. Introduction

The performance of radio reception of SDARS satellite radio is increased drastically by using antenna diversity. This is true not only for the prevention of shadowing effects but also for the very common problem of Rayleigh-fading which occurs especially at locations with trees of dense foliage. The system is able to check several antennas and aquire the signals, judge them level and switch to the best antenna with the best signal detected. An important delay time constant is introduced by the three modules of the system: signal detection, control unit and antenna switcher. The simple detection of the signal level isn't satisfactory it's noisy and unstable for a time period that the control unit needs to do the conversion.

2. Analysis.

The detection part of the antenna diversity system is used as reference of the switching logic algorithm. If the DC output signal from the detection module is aleatory variable the analog/digital conversion often isn't real and due to that the system will commute to the wrong antenna. The conversion process needs a time

period which depends on the control unit time conversion. That means that for whole conversion period the value obteined after detection has to be hold. Talking about the level after the primary detection it's small and the variation level is almost undistinguishable.

By a integration of the detected signal during a time period the level is increasing and get stabilty. In the end of the integration time it has been held during the conversion time.

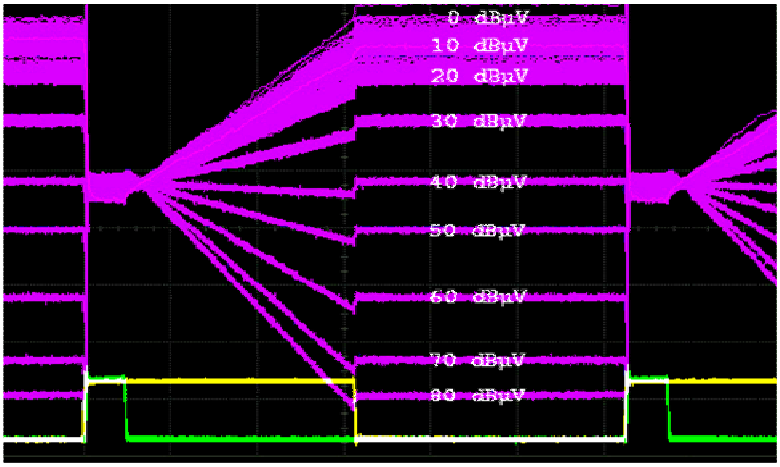

Figure 1. The DC output variation diagram at 21.4 MHz, for input signal range 0 to 80 dBµV

In this way a more complex detection circuit was obtained, which is based on two different circuits:

1. The proper Detection Circuit and
2. the Integration Circuit.

The primary detection is realized with the detection module contained in the TDA1576T integrated circuit, which is a FM/IF amplifier/demodulator circuit. The output signal is unfortunately noisy and has a low dynamic range.

For integration realisation we use a sample and hold amplifier type built from discrete components.

The circuit is realised as follows:

- three AD8055AN ICs, using them as pulse and signal amplifiers;
- two SST310 SMD transistors for switching the signal;
- dual retriggerable monostable multivibrator with reset MM74HC123AN.

This Detection Circuit is not stable in every case, the output voltage variation range 0-2.5 V is not big enough and the integration period takes too time. The problem is partially due to the TDA1576T which does not include gain stages and only does a simple detection.

3. Exemples for improveing of the first design

The new detection circuit is based on the 92 dBm logarithmic amplifier AD8307, it is easy to use due to the fact that it requires little external components in a simple schematic and could be used without adjusting elements. It was observed that the signal level evolution is significant and the noise was less than in the case of the TDA1576T, while signal stability is very good up to an input signal level of -70 dBm towards 0 dBm; after that output signal quality does not get worse.

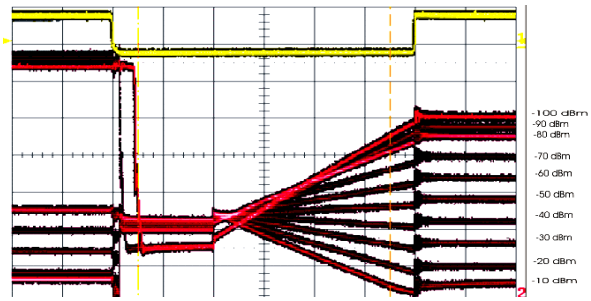

Figure 2. The DC output variation diagram at 21.4 MHz, for input signal range -100 to -10 dBm

In Figure 2, after the Integration process, the DC output voltage variation covers the whole 0-5 V range needed for increasing the switching precision. Also, due to the AD8307 DC output stabilty, the integration time has been decreased.

Two HA5320, witch is a Sample & Hold specialised IC, have been used to do the sample and hold processes separately in order to achieve a shorter integration time Figure 3.

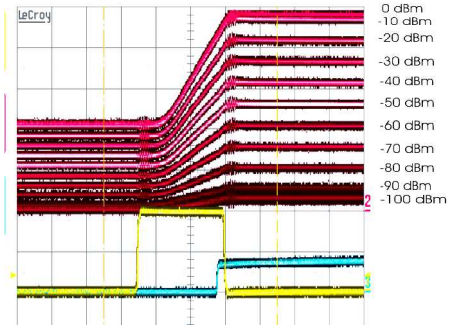

Figure 3.

4. Conclusion

The Detection Circuit obtained has a good stability and the evolution of the output DC voltage is almost linear. The range of output voltage is enough width for both of the frequencies. On the other hand, due to the internal capacity, the HA5320 IC does a small amplitude for the proper integration process and the gain of the AD8055AN is important. Therefore the DC output voltage is noisy. Otherwise the response to a small integration time is better. A very good performance could be achieved if another IC will be find, with no- or smaller internal capacity, at least for the integration process.

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